98. (New) The method in claim 97, wherein said incorporating act comprises incorporating said memory device into said computer system after said testing act.

99. (New) A method of repairing a plurality of memory die, comprising:

replacing a first plurality of memory cells of one memory die with a second plurality of memory cells;

storing on said one memory die at most a partial address common to said second plurality of memory cells;

replacing a third plurality of memory cells of another memory die with a fourth plurality of memory cells; and

storing on said another memory die at most a partial address common to said fourth plurality of memory cells.

100. (New) The method in claim 99, further comprising locating said one memory die and said another memory die on a tester during said acts of replacing a first plurality and replacing a third plurality.

101. (New) The method in claim 99, further comprising:

singulating said one memory die and said another memory die;

establishing electrical communication between a common component and said one memory die;

establishing electrical communication between said common component and said another memory die; and

testing said one memory die and said another memory die using said common component.

102. (New) The method in claim 101, wherein said act of establishing electrical communication between a common component and said one memory die comprises establishing electrical communication between a tester and said one memory die.

103. (New) The method in claim 101, further comprising at least partially packaging said one memory die before said testing act.

104. (New) The method in claim 103, further comprising fully packaging said one memory die and said another memory die before said testing act.

105. (New) A signaling method for a plurality of semiconductor devices, comprising:

transmitting a plurality of signals to said plurality of semiconductor devices, wherein said plurality of signals includes a pulsed signal;

logically relating said plurality of signals on each semiconductor device of said plurality of semiconductor devices; and

generating an output signal on said each semiconductor device, wherein said output signal results from said act of logically relating, and wherein said output signal pulses less frequently than said pulsed signal.

106. (New) The method in claim 105, wherein said act of transmitting comprises transmitting said plurality of signals from a tester.

107. (New) The method in claim 105, wherein:

said method further comprises mounting said plurality of semiconductor devices on a common substrate; and

said act of transmitting comprises transmitting said plurality of signals through said substrate.

108. (New) The method in claim 107, further comprising including said substrate as part of an AMBYX testing device.